

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|-------------|--|--|---------------------|
| 1 | BRS | L1 | 159439 9 | planar\$6 or preplanar\$6 or CPM or flat\$6 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:27 |
| 2 | BRS | L2 | 780386 | bump\$3 or ball\$3 or BGA | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:28 |
| 3 | BRS | L3 | 19066 | 1 near8 2 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:28 |
| 4 | BRS | L4 | 107652 | reflow\$4 or reconstitut\$4 or reform\$4 or reshap\$4 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:30 |
| 5 | BRS | L5 | 4537 | 4 near4 2 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:30 |

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|---|------|-----|------|-----------------|--|---------------------|
| 6 | BRS | L6 | 259 | 3 same 5 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 11:30 |
| 7 | BRS | L7 | 291 | 1 with 2 with 4 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 15:53 |
| 8 | BRS | L8 | 103 | 7 not 6 | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B | 2003/09/17 15:53 |

US-PAT-NO: 6400021

DOCUMENT-IDENTIFIER: US 6400021 B1

TITLE: Wafer level package and method for
fabricating the same

----- KWIC -----

Detailed Description Text - DETX (13):

Next, as shown in FIG. 11, the solder ball 60 is put on the ball land 51, and then the solder ball 60 is firmly adhered to the ball land 51 through a reflow process by means of ultraviolet rays. In this case, the portion of the metal pattern 41 with which the solder ball 60 is in contact does not have a simple flat shape as that in the prior art, but has an uneven shape.

Accordingly, the solder ball 60 is inserted in the grooves 32 also, so that the contact area between the solder ball 60 and the metal pattern 41 is enlarged by a degree corresponding to the length of the inner wall of the grooves 32.

Especially, since the bottom surface of the grooves 32 is formed of a silicon nitride film, and since the solder ball 60 is directly in contact with the nitride film 20, the adhesion force is largely strengthened in comparison with the case where the solder ball is in contact with the metal layer.

DOCUMENT-IDENTIFIER: US 20030057565 A1

TITLE: Making interconnections to a
non-flat surface

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Abstract Paragraph - ABTX (1):

A non-planar surface may be surface mounted to another surface using solder balls that may be modified to generate a planar surface for receiving the second surface. In one embodiment, the solder balls may be secured to an irregular surface and then scrapped to form a planar contacting surface. A second surface to be bonded to the first surface may then be attached to the planar contacting surface and the solder balls reflowed to create a surface mount.

Summary of Invention Paragraph - BSTX (6):

[0005] Generally, the two surfaces to be bonded may be relatively flat but need not be perfectly flat. When a typical solder bumped flip-chip is attached to a circuit board by reflowing the solder, the solder bumps collapse or flatten to some degree, as a result of wetting of the solder to the bonding pad of the circuit board. This collapse may accommodate some variation in the bump height and good electrical connections can be made even with variations in bump height of about 1 mil, the normal height being 4 mils. Thus, flip-chip bump suppliers routinely supply bumped devices that meet this requirement of bump height tolerance.

US-PAT-NO: 6109507

DOCUMENT-IDENTIFIER: US 6109507 A

TITLE: Method of forming solder bumps and
method of forming preformed solder bumps

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Detailed Description Text - DETX (15):

In the above-described reflow process, the organic flux in the solder paste 22 may evaporate and solder particles may fuse so as to form a lower solder bump layer 30A (see FIG. 10). Note that immediately after the reflow process, the lower solder bump layer 30A has a spherical shape due to the surface tension which has acted during fusion of the solder particles. Accordingly, the lower solder bump layer 30A thus formed will be subjected to a flattening step (step 14 in FIG. 5).

DOCUMENT-IDENTIFIER: US 20020173135 A1

TITLE: Bump transfer plate, manufacturing
method thereof,
semiconductor device, and
manufacturing method thereof

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Detail Description Paragraph - DETX (18):

[0073] In addition, when the semiconductor device is formed, the contact surface 12b of the solder bump 12 with the base 13 is flat, and the electrode 7 is pressed against the solder bump 12 prior to the reflow, and, therefore, a flat part 12e is formed in the solder bump 12 after the reflow. Therefore, there is no need to beforehand allow the solder bump 12 to undergo coining before the solder bump 12 is bonded to the land 5 of the package substrate 2. Therefore, the labor required for manufacturing can be reduced. In other words, the semiconductor device can be manufactured easily and efficiently.

DOCUMENT-IDENTIFIER: US 20020151164 A1

TITLE: Structure and method for depositing
solder bumps on a
wafer

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Summary of Invention Paragraph - BSTX (12):

[0010] In another embodiment for the article, the article includes a substrate; a conductive layer disposed on the substrate; and a first solder bump having an abraded or severed internal planar surface and disposed on the conductive region. The article includes a dielectric layer having a top surface and positioned on the substrate and a diffusion barrier placed on the abraded or severed internal planar surface. The article further includes a second solder bump disposed on the diffusion barrier. The abraded or severed internal planar surface is disposed below the top surface of the dielectric layer at a defined distance therefrom. Preferably, the diffusion barrier comprises a thickness having a value generally equal to the defined distance, and the first solder bump has a higher reflow temperature than a reflow temperature of the second solder bump which includes an exterior surface that generally terminates at a juncture point of a top barrier surface of diffusion barrier and the top surface of the dielectric layer. The top barrier surface is generally aligned with the top surface of the dielectric layer.

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| 1 | IS&R | L1 | 2299 | (438/106).CCLS. | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B |
| 2 | IS&R | L2 | 870 | (438/127).CCLS. | USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B |